BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of: Lukanc et al.

Serial No.: 10/790,590

Filed: March 1, 2004

Group Art Unit: 2825

Before the Examiner: Whitmore, Stacy

Title: SYSTEM AND METHOD FOR DESIGNING AN INTEGRATED CIRCUIT DEVICE

APPEAL BRIEF

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

I. REAL PARTY IN INTEREST

The real party in interest is Advanced Micro Devices, Inc., which is the assignee of the entire right, title and interest in the above-identified patent application.

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to Appellants, Appellants' legal representative or assignee which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 1-4, 6-20 and 31 are pending in the Application. Claims 5 and 21-30 were cancelled. Claims 1-4, 6-20 and 31 stand rejected. Claims 1-4, 6-20 and 31 are appealed.

IV. STATUS OF AMENDMENTS

Appellants have not submitted any amendments following receipt of the final rejection with a mailing date of October 23, 2006.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Independent Claim 1:

In one embodiment of the present invention, a method of designing an integrated circuit (IC) device having desired electrical characteristics comprising the step of providing an initial IC device design. Specification, page 7, lines 17-25; Figure 3, step 300. The method further comprises generating a layout representation corresponding to the initial IC device design. Specification, page 7, line 26 – page 8, line 14; Figure 3, step 310. The method further comprises simulating how structures within the layout representation will pattern on a wafer. Specification, page 8, lines 15-25; Figure 3, step 320. The method further comprises based on the simulating step, determining whether actual electrical characteristics associated with the initial IC device design sufficiently match the desired electrical characteristics, where the desired electrical characteristics include at least one of gain and switching speed. Specification, page 8, line 26 – page 9, line 32; Figure 3, steps 340, 350. The method further comprises that if the actual electrical characteristics associated with the initial IC device design do not sufficiently match the desired electrical characteristics, modifying the initial IC device design. Specification, page 10, lines 1-9; Figure 3, step 360.

Independent Claim 31:

In one embodiment of the present invention, a computer-implemented method in which an initial integrated circuit (IC) device design is provided, the method comprising generating a layout representation corresponding to the initial IC device design. Specification, page 6, line 4 – page 7, line 16; Specification, page 7, line 26 – page 8, line 14; Figure 2, element 200; Figure 3, step 310. The method further

comprises simulating how structures within the layout representation will pattern on a wafer. Specification, page 6, line 4 – page 7, line 16; Specification, page 8, lines 15-25; Figure 2, element 200; Figure 3, step 320. The method further comprises based on the simulating step, determining an amount of process-related variation in how at least a portion of the layout representation will pattern on a wafer. Specification, page 6, line 4 – page 7, line 16; Specification, page 8, line 26 – page 9, line 4; Figure 2, element 200; Figure 3, step 330. The method further comprises determining whether the layout representation will pattern as an IC device having desired electrical characteristics, where the desired electrical characteristics include at least one of gain and switching speed. Specification, page 6, line 4 – page 7, line 16; Specification, page 9, lines 5-32; Figure 2, element 200; Figure 3, steps 340, 350.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Claims 1-4, 6-9, 12-18, 20 and 31 stand rejected under 35 U.S.C. §103(a) as being unpatentable over White et al. (U.S. Patent Application Publication No. 2003/0229868) (hereinafter "White") in view of Hatsch (U.S. Patent No. 6,735,742).

B. Claims 10-11 and 19 stand rejected under 35 U.S.C. §103(a) as being unpatentable over White in view of Hatsch and in further view of Rosenbluth et al. (U.S. Patent Application Publication No. 2002/0140920) (hereinafter "Rosenbluth").

VII. ARGUMENT

A. Claims 1-4, 6-9, 12-18, 20 and 31 are improperly rejected under 35 U.S.C. §103(a) as being unpatentable over White in view of Hatsch.

The Examiner rejects claims 1-4, 6-9, 12-18, 20 and 31 under 35 U.S.C. §103(a) as being unpatentable over White in view of Hatsch. Office Action (10/23/2006), page 2. Appellants respectfully traverse these rejections for at least the reasons stated below.

1. Examiner's motivation for modifying White with Hatsch to include the missing claim limitation of claims 1 and 31 is insufficient to establish a *prima facie* case of obviousness.

Most if not all inventions arise from a combination of old elements. *See In re Rouffet*, 47 U.S.P.Q.2d 1453, 1457 (Fed. Cir. 1998). Obviousness is determined from the vantage point of a hypothetical person having ordinary skill in the art to which the patent pertains. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1457 (Fed. Cir. 1998). Therefore, an Examiner may often find every element of a claimed invention in the prior art. *Id.* However, identification in the prior art of each individual part claimed is insufficient to defeat patentability of the whole claimed invention. *See Id.* In order to establish a *prima facie* case of obviousness, the Examiner must show reasons that the skilled artisan, confronted with the same problems as the inventor and with no knowledge of the claimed invention, would select the elements from the cited prior art references for combination in the manner claimed. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1458 (Fed. Cir. 1998). That is, the Examiner must provide some suggestion or motivation, either in the references themselves, the knowledge of one of ordinary skill in the art, or, in some case, the nature of the problem to be solved, to modify the reference or to combine reference teachings. *See In re Dembiczak*, 175 F.3d 994, 999, 50 U.S.P.Q.2d 1614, 1617 (Fed. Cir. 1999). Whether the Examiner relies on an express or an implicit showing, the Examiner must provide particular findings related thereto. *In re Kotzab*, 55 U.S.P.Q.2d 1313, 1317 (Fed. Cir. 2000).

The Examiner admits that White does not teach "wherein the desired electrical characteristics include at least one of gain and switching speed" as recited in claim 1 and similarly in claim 31. Office Action (10/23/2006), page 6. The Examiner asserts that Hatsch teaches the above-cited claim limitation. *Id.* The Examiner's motivation for modifying White with Hatsch to include the above-cited claim limitation is to "optimize[ing] layouts for functional capability and desired requirements concerning critical paths which would improve design and circuit performance [see Hatsch, col. 3, especially lines 1-16, and 43-51]." Office Action (10/23/2006, page 6). The

Examiner's motivation is insufficient to establish a *prima facie* case of obviousness in rejecting claims 1-4, 6-20 and 31.

The Examiner' motivation ("to optimize layouts for functional capability and desired requirements concerning critical paths which would improve design and circuit performance") does not provide reasons, as discussed further below, that the skilled artisan, confronted with the same problems as the inventor and with no knowledge of the claimed invention, would modify White to include the above-indicated missing claim limitation of claims 1 and 31. Accordingly, the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 1-4, 6-20 and 31. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1458 (Fed. Cir. 1998).

As stated above, the Examiner cites column 3 of Hatsch as support for the Examiner's motivation. Hatsch teaches using parameters, such as power, area and speed, to determine critical paths. Column 3, lines 27-33. Hatsch further teaches that the critical path is an electrical conductor or signal path between a specific input of the circuit and an output of the circuit which turns out to be the worst signal path according to predetermined optimization parameters. Column 3, lines 33-36. Hence, Hatsch teaches identifying a critical path using parameters, such as power, area and speed, where the critical path is the worst signal path.

White, on the other hand, addresses the problem of reducing variations in fabricated chips. [0002-0004]. The Examiner has not provided any reasons as to why one skilled in the art would modify White (which teaches reducing variations in fabricated chips) to determine whether actual electrical characteristics associated with the initial IC design sufficiently match the desired electrical characteristics, where the desired electrical characteristics include at least one of gain and switching speed (missing claim limitation). The Examiner's motivation ("to optimize layouts for functional capability and desired requirements concerning critical paths which would improve design and circuit performance") does not provide such reasoning.

Why would the reason to modify White (whose purpose is to reduce variations in fabricated chips) to determine whether actual electrical characteristics associated with the initial IC design sufficiently match the desired electrical characteristics, where the desired electrical characteristics include at least one of gain and switching speed (missing claim limitation) be to identify a critical path using parameters, such as power, area and speed, where the critical path is the worst signal path? White is not concerned with identifying a critical path. The Examiner cannot completely ignore the teachings of White in concluding it would have been obvious to modify White with Hatsch to include the missing claim limitation of claims 1 and 31.[1] The Examiner is simply citing to a passage in Hatsch which supports reasons for why Hatsch using speed as a parameter in identifying a critical path. How does this relate as to why one skilled in the art would modify White (whose purpose is to reduce variations in fabricated chips) to determine whether actual electrical characteristics associated with the initial IC design sufficiently match the desired electrical characteristics, where the desired electrical characteristics include at least one of gain and switching speed (missing claim limitation)? Hence, the Examiner's motivation does not provide reasons that the skilled artisan, confronted with the same problems

1 Appellants respectfully request Examiner Whitmore to respond to the following example. For example, suppose that the invention of a super soaker gun (essentially a plastic gun that shoots water) was never developed and an Applicant filed for a patent application on the super soaker gun. Applicant claims a plastic gun with a container of water that shoots water. The Examiner cites a primary reference that teaches a plastic gun that shoots darts and cites a secondary reference that teaches a plastic toy that contains a container of water. Since the primary reference does not teach a container filled with water, the Examiner cites the secondary reference as teaching this missing claim limitation. The secondary reference specifically states that the purpose of the container is to carry water. The Examiner then concludes that it would have been obvious to modify the primary reference with the secondary reference in order to carry water. The Examiner believes that he/she has established a *prima facie* case of obviousness since the Examiner has found a reason to have a container of water. However, the Examiner is completely ignoring the teaching of the primary reference. Why would one skilled in the art modify a plastic gun that shoots darts to have a container of water? This is the key question to answer. While having a container of water may be used to carry water, that is irrelevant as far as the purpose of the primary reference. Simply citing to a passage in the secondary reference that discusses the purpose of that secondary reference may not be sufficient evidence for an obviousness rejection. After all, surely there is a reason as to why the secondary reference teaches the missing claim limitation or else why would it include it? The Examiner must explain the connection between the teachings of the primary reference and the rationale of the secondary reference for including the missing claim limitation. Otherwise, everything can be deemed obvious and virtually nothing can be patented.

as the inventor and with no knowledge of the claimed invention, would modify White to include the missing claim limitation of claims 1 and 31. Accordingly, the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 1-4, 6-20 and 31. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1458 (Fed. Cir. 1998).

2. White and Hatsch, taken singly or in combination, do not teach or suggest the following claim limitations.

a. Claim 3 is patentable over White in view of Hatsch.

Appellant respectfully asserts that White and Hatsch, taken singly or in combination, do not teach or suggest "wherein the actual electrical characteristics associated with the actual dimensions of the structures within the layout representation are determined using a look-up table" as recited in claim 3. The Examiner cites paragraph [0211] of White as teaching the above-cited claim limitation. Office Action (10/23/2006), page 3. Appellants respectfully traverse and assert that White instead teaches that the layout for the current design level is loaded and a table is assembled that maps layout features to discrete grids in chip surface topography prediction. [0211]. White further teaches that conventional optical proximity algorithms, many of which are commercially available in EDA tools, are used to map feature density to feature dimension variation 644. [0211]. Hence, White teaches loading a currently design level and assembling a table that maps layout features to discrete grids in chip surface topography prediction. There is no language in the cited passage that teaches that the actual electrical characteristics associated with the actual dimensions of the structures within the layout representation are determined using a look-up table. Therefore, the Examiner has not presented a *prima facie* case of obviousness in rejecting claim 3, since the Examiner is relying upon incorrect, factual predicates in support of the rejection. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1455 (Fed. Cir. 1998).

b. Claim 4 is patentable over White in view of Hatsch.

Appellants respectfully assert that White and Hatsch, taken singly or in combination, do not teach or suggest "wherein the actual electrical characteristics associated with the actual dimensions of the structures within the layout representation are determined using an electrical modeling program in which the actual dimensions of the structures are input" as recited in claim 4. The Examiner cites paragraphs [0047, 0140 and 0147] of White as teaching the above-cited claim limitation. Office Action (10/23/2006), page 3. Appellants respectfully traverse.

White instead teaches Figure 21B illustrates a continuation of the steps in prediction of chip topography. [0047]. White further teaches that one option to use models in which the lithography process flow 600 is defined to include not only the lithography process step buy may also include pre and post photoresist deposition and subsequent plasma etch. [0140]. White additionally teaches that this may be useful if the actual physical feature dimensions are desired, as an alternative to the patterned feature dimensions that lithography models alone provide. [0140]. White further teaches that the difference between the two approaches is that in mode A, the design is modified before mask creation and tape-out to produce the desired dimensions and thus the original design and extraction reflect the actual printed circuit dimensions. [0147]. Hence, White teaches that including pre and post photoresist deposition and subsequent plasma etch in the lithography process flow may be useful if the actual physical feature dimensions are desired. There is no language in the cited passages that teaches determining actual electrical characteristics. Neither is there any language in the cited passages that teaches that the actual electrical characteristics associated with the actual dimensions of the structures within the layout representation are determined using an electrical modeling program in which the actual dimensions of the structures are input. Therefore, the Examiner has not presented a *prima facie* case of obviousness in rejecting claim 4, since the Examiner is relying upon incorrect, factual predicates in support of the rejection. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1455 (Fed. Cir. 1998).

c. Claim 6 is patentable over White in view of Hatsch.

Appellants respectfully assert that White and Hatsch, taken singly or in combination, do not teach or suggest "wherein the step of generating a layout representation corresponding to the initial IC device design includes minimizing the scale of the layout representation" as recited in claim 6. The Examiner cites paragraph [0009] of White as teaching the above-cited claim limitation. Office Action (10/23/2006), page 3. Appellants respectfully traverse and assert that White instead teaches that generation is performed on sub-portions of the circuit. [0009]. There is no language in the cited passage that teaches that the step of generating a layout representation corresponding to the initial IC device design includes minimizing the scale of the layout representation. Therefore, the Examiner has not presented a *prima facie* case of obviousness in rejecting claim 6, since the Examiner is relying upon incorrect, factual predicates in support of the rejection. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1455 (Fed. Cir. 1998).

d. Claim 7 is patentable over White in view of Hatsch.

Appellants respectfully assert that White and Hatsch, taken singly or in combination, do not teach or suggest "wherein the initial IC device design includes a desired relationship between at least two structures within the IC device design" as recited in claim 7. The Examiner cites paragraph [0115] of White as teaching the above-cited claim limitation. Office Action (10/23/2006), page 3. Appellants respectfully traverse and assert that White instead teaches that an integrated circuit typically includes multiple levels of materials that have been deposited, planarized, and selectively etched to reproduce circuitry defined by a computer-generated design. [0115]. White further teaches that lithography is a frequently repeated process step during the manufacture of ICs in which a pattern that defines the dimensions of the circuitry is transferred to a silicon wafer. [0115]. There is no language in the cited passage that teaches that the initial IC device design includes a desired relationship between at least two structures within the IC device design. Therefore, the Examiner

has not presented a *prima facie* case of obviousness in rejecting claim 7, since the Examiner is relying upon incorrect, factual predicates in support of the rejection. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1455 (Fed. Cir. 1998).

e. Claim 8 is patentable over White in view of Hatsch.

Appellants respectfully assert that White and Hatsch, taken singly or in combination, do not teach or suggest "determining an amount of process-related variation associated with at least two structures within the layout representation of the IC device design" as recited in claim 8. The Examiner cites paragraphs [0112-0115] of White as teaching the above-cited claim limitation. Office Action (10/23/2006), page 4. Appellants respectfully traverse.

White instead teaches approaches that are useful to identify and correct areas of integrated circuit that are likely to be problematic due to variations in film thickness, surface topography uniformity, and electrical impact that arise in the manufacture of an integrated circuit. [0112]. White further teaches that in fabricating integrated circuits, the degree of interconnect film uniformity is dependent on characteristics of circuit layout patterns. [0114]. White additionally teaches that an integrated circuit typically includes multiple levels of materials that have been deposited, planarized, and selectively etched to reproduce circuitry defined by a computer-generated design. [0115]. White further teaches that lithography is a frequently repeated process step during the manufacture of ICs in which a pattern that defines the dimensions of the circuitry is transferred to a silicon wafer. [0115]. There is no language in the cited passages that teaches determining an amount of process-related variation associated with at least two structures within the layout representation of the IC device design. Therefore, the Examiner has not presented a *prima facie* case of obviousness in rejecting claim 8, since the Examiner is relying upon incorrect, factual predicates in support of the rejection. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1455 (Fed. Cir. 1998).

f. Claim 12 is patentable over White in view of Hatsch.

Appellants respectfully assert that White and Hatsch, taken singly or in combination, do not teach or suggest "measuring the feature indicative of process-related variation for one or more simulated structures over a process window of focus and intensity" as recited in claim 12. The Examiner cites paragraphs [0120, 0121 and 0306] of White as teaching the above-cited claim limitation. Office Action (10/23/2006), page 4. Appellants respectfully traverse and assert that White instead teaches that while the stepper can account for die-to-die variation, it may not adequately address within-die variation caused by IC pattern dependencies. [0120]. White further teaches that during deposition of copper material via ECD or through the CMP of oxide or copper, for example, process related pattern dependencies often cause within-die variation 30 across the chip. [0121]. White additionally teaches that the results of a layout extraction using the system are shown in the images in FIGS. 60A and 60B. [0306]. White further teaches that FIG. 60A shows a full-chip image 3167 of extracted feature widths across the chip according to the scale shown the right 3168. [0306]. There is no language in the cited passages that teaches measuring the feature indicative of process-related variation for one or more simulated structures over a process window of focus and intensity. Therefore, the Examiner has not presented a *prima facie* case of obviousness in rejecting claim 12, since the Examiner is relying upon incorrect, factual predicates in support of the rejection. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1455 (Fed. Cir. 1998).

g. Claim 14 is patentable over White in view of Hatsch.

Appellants respectfully assert that White and Hatsch, taken singly or in combination, do not teach or suggest "wherein simulating how structures within the layout representation will pattern on a wafer includes simulating how structures within the layout representation will pattern as a function of at least one of (i) proximity of a structure to other structures, (ii) density of structures within a portion of the IC device design, (iii) orientation of a structure, (iv) placement of a structure

within a portion of the IC device design, and (v) size of a structure with respect to other adjacent structures" as recited in claim 14. The Examiner cites paragraphs [0168 and 0211] of White as teaching density of structures within a portion of the IC device design and cites paragraph [0211] of White as teaching size of a structure with respect to other adjacent structures. Office Action (10/23/2006), page 4. Appellants respectfully traverse.

White instead teaches that during or after the physical verification step in a design flow, the design may be passed through the optical proximity correction to adapt the design file used to create masks with regard to feature density. [0168]. While White teaches adapting the design file with regard to feature density, there is no language in the cited passages that teaches simulating how structures within the layout representation will pattern as a function of the density of structures <u>within a portion</u> of the IC device design.

Further, White instead teaches that the layout for the current design level is loaded and a table is assembled that maps layout features to discrete grids in chip surface topography prediction. [0211]. There is no language in the cited passages that teaches simulating how structures within the layout representation will pattern as a function of the size of a structure <u>with respect to other adjacent structures</u>.

Therefore, the Examiner has not presented a *prima facie* case of obviousness in rejecting claim 14, since the Examiner is relying upon incorrect, factual predicates in support of the rejection. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1455 (Fed. Cir. 1998).

h. <u>Claim 17 is patentable over White in view of Hatsch.</u>

Appellants respectfully assert that White and Hatsch, taken singly or in combination, do not teach or suggest "wherein modifying at least a portion of the IC device design includes modifying at least one of (i) proximity of a structure to other structures, (ii) density of structures within a portion of the IC device design, (iii)

orientation of a structure, and (ii) (iv) placement of a structure within a portion of the IC device design, and (v) size of a structure with respect to other adjacent structures" as recited in claim 17. The Examiner cites paragraph [0142] of White as teaching modifying the density of structures within a portion of the IC device design as well as teaching modifying the size of a structure with respect to other adjacent structures. Office Action (10/23/2006), page 5. Appellants respectfully traverse.

White instead teaches that the predicted feature dimension variation 680 and the desired feature dimension specification and tolerances 750 are input into a verification and correction component 800 which identifies any features that will exceed or approach the tolerances. [0141]. White further teaches that once these modifications are made to the IC design, dummy fill may be reinserted or adjusted and a new layout generated. [0141]. White explains that dummy fill is a method of improving film thickness uniformity in integrated circuits through the addition of the structures or the removal of existing structures. [0142]. Hence, White teaches that after modifications are made to the IC design, dummy fill may be reinserted or adjusted where dummy fill improves film thickness uniformity. There is no language in the cited passage that teaches that if a portion of the IC device design is not optimized with respect to process-related variations, then a portion of the IC device design is modified by modifying the density of structures within a portion of the IC device design. Instead, White teaches that dummy fill may be reinserted or adjusted to improve film thickness uniformity after modifications are made. Further, there is no language in the cited passage that teaches that if a portion of the IC device design is not optimized with respect to process-related variations, then a portion of the IC device design is modified by modifying the size of a structure with respect to other adjacent structures. Therefore, the Examiner has not presented a *prima facie* case of obviousness in rejecting claim 17, since the Examiner is relying upon incorrect, factual predicates in support of the rejection. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1455 (Fed. Cir. 1998).

i. Claim 18 is patentable over White in view of Hatsch.

Appellants respectfully assert that White and Hatsch, taken singly or in combination, do not teach or suggest "wherein the process-related variations include variations caused by at least one of (i) mask generation, (ii) wafer patterning, (iii) pre-patterning processing, and (iv) post-patterning processing" as recited in claim 18. The Examiner cites paragraph [0112] of White as teaching mask generation. Office Action (10/23/2006), page 5. Appellants respectfully traverse.

White instead teaches describing approaches that are useful to identify and correct areas of integrated circuit that are likely to be problematic due to variations in film thickness, surface topography uniformity, and electrical impact that arise in the manufacture of an integrated circuit. [0112]. There is no language in the cited passage that teaches that the process-related variations include variations caused by at least one of (i) mask generation, (ii) wafer patterning, (iii) pre-patterning processing, and (iv) post-patterning processing. Therefore, the Examiner has not presented a *prima facie* case of obviousness in rejecting claim 18, since the Examiner is relying upon incorrect, factual predicates in support of the rejection. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1455 (Fed. Cir. 1998).

B. Claims 10-11 and 19 are improperly rejected under 35 U.S.C. §103(a) as being unpatentable over White in view of Hatsch and in further view of Rosenbluth.

The Examiner rejects claims 10-11 and 19 under 35 U.S.C. §103(a) as being unpatentable over White in view of Hatsch and in further view of Rosenbluth. Office Action (10/23/2006), page 6. Appellants respectfully traverse these rejections for at least the reasons stated below.

1. Examiner's motivation for modifying White with Rosenbluth to include the missing claim limitations of claims 10 and 11 is insufficient to establish a *prima facie* case of obviousness.

As stated above, most if not all inventions arise from a combination of old elements. *See In re Rouffet*, 47 U.S.P.Q.2d 1453, 1457 (Fed. Cir. 1998). Obviousness is determined from the vantage point of a hypothetical person having ordinary skill in the art to which the patent pertains. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1457 (Fed. Cir. 1998). Therefore, an Examiner may often find every element of a claimed invention in the prior art. *Id.* However, identification in the prior art of each individual part claimed is insufficient to defeat patentability of the whole claimed invention. *See Id.* In order to establish a *prima facie* case of obviousness, the Examiner must show reasons that the skilled artisan, confronted with the same problems as the inventor and with no knowledge of the claimed invention, would select the elements from the cited prior art references for combination in the manner claimed. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1458 (Fed. Cir. 1998). That is, the Examiner must provide some suggestion or motivation, either in the references themselves, the knowledge of one of ordinary skill in the art, or, in some case, the nature of the problem to be solved, to modify the reference or to combine reference teachings. *See In re Dembiczak*, 175 F.3d 994, 999, 50 U.S.P.Q.2d 1614, 1617 (Fed. Cir. 1999). Whether the Examiner relies on an express or an implicit showing, the Examiner must provide particular findings related thereto. *In re Kotzab*, 55 U.S.P.Q.2d 1313, 1317 (Fed. Cir. 2000).

The Examiner admits that White does not teach "wherein the feature indicative of process-related variation is at least one of (i) slope of edge intensity and (ii) logarithm of slope of edge intensity" as recited in claim 10. Office Action (10/23/2006), page 7. The Examiner further admits that White does not teach "a larger slope of edge intensity or logarithm of slope of edge intensity is indicative of a smaller process-related variation; and a smaller slope of edge intensity or logarithm of slope of edge intensity is indicative of a larger process-related variation" as recited in claim 11. *Id.* The Examiner asserts that Rosenbluth teaches the above-cited claim limitations. *Id.* The Examiner's motivation for modifying White with Rosenbluth to include the above-cited claim limitations is "because such combined method includes

slope of edge intensity/logarithm of slope of edge intensity would provide a technique for optimally choosing illumination distribution and mask features (paragraph [0021]." *Id.* The Examiner's motivation is insufficient to establish a *prima facie* case of obviousness in rejecting claims 10-11 and 19.

The Examiner' motivation ("to provide a technique for optimally choosing illumination distribution and mask features") does not provide reasons, as discussed further below, that the skilled artisan, confronted with the same problems as the inventor and with no knowledge of the claimed invention, would modify White to include the above-indicated missing claim limitations of claims 10-11. Accordingly, the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 10-11 and 19. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1458 (Fed. Cir. 1998).

As stated above, the Examiner cites paragraph [0021] of Rosenbluth as support for the Examiner's motivation. Rosenbluth teaches that it is an <u>object of the present invention to provide a method for optimally choosing illumination distribution and reticle mask features so that the number of adjustable degrees of freedom per resolution element is significantly increased</u>. [0021]. There is no language in Rosenbluth (and in particular paragraph [0021]) that makes any suggestion that the feature indicative of process-related variation be at least one of (i) slope of edge intensity and (ii) logarithm of slope of edge intensity or that a larger slope of edge intensity or logarithm of slope of edge intensity be indicative of a smaller process-related variation; and a smaller slope of edge intensity or logarithm of slope of edge intensity be indicative of a larger process-related variation (missing claim limitations) so that the number of adjustable degrees of freedom per resolution element is significantly increased. The Examiner has simply cited to an arbitrary passage in Rosenbluth that mentions some benefit caused by the invention of Rosenbluth and then concludes that the Examiner has provided appropriate motivation. <u>The Examiner has to provide some rationale connection between the cited passage that is the source of the motivation and the missing claim limitations.</u>

The Examiner's source of motivation (paragraph [0021] of Rosenbluth) does not provide reasons as to why one skilled in the art would modify White to include the missing claim limitations of claims 10-11. Accordingly, the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 10-11 and 19. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1458 (Fed. Cir. 1998).

Further, White addresses the problem of reducing variations in fabricated chips. [0002-0004]. The Examiner has not provided any reasons as to why one skilled in the art would modify White (which teaches reducing variations in fabricated chips) to have the feature indicative of process-related variation be at least one of (i) slope of edge intensity and (ii) logarithm of slope of edge intensity and to have a larger slope of edge intensity or logarithm of slope of edge intensity be indicative of a smaller process-related variation; and a smaller slope of edge intensity or logarithm of slope of edge intensity be indicative of a larger process-related variation (missing claim limitations). The Examiner's motivation ("to provide a technique for optimally choosing illumination distribution and mask features") does not provide such reasoning.

Why would the reason to modify White (whose purpose is to reduce variations in fabricated chips) to have the feature indicative of process-related variation be at least one of (i) slope of edge intensity and (ii) logarithm of slope of edge intensity and to have a larger slope of edge intensity or logarithm of slope of edge intensity be indicative of a smaller process-related variation; and a smaller slope of edge intensity or logarithm of slope of edge intensity be indicative of a larger process-related variation (missing claim limitations) be to provide a technique for optimally choosing illumination distribution and mask features? White is not concerned with optimally choosing illumination distribution and mask features. The Examiner cannot completely ignore the teachings of White in concluding it would have been obvious to modify White with Rosenbluth to include the missing claim limitations of claims 10-11. Further, what is the rationale connection between the missing claim

limitations and optimally choosing illumination distribution and mask features? Hence, the Examiner's motivation does not provide reasons that the skilled artisan, confronted with the same problems as the inventor and with no knowledge of the claimed invention, would modify White to include the missing claim limitations of claims 10-11. Accordingly, the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 10-11 and 19. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1458 (Fed. Cir. 1998).

2. White, Hatsch and Rosenbluth, taken singly or in combination, do not teach or suggest the following claim limitations.

a. Claim 10 is patentable over White in view of Hatsch and in further view of Rosenbluth.

Appellants respectfully assert that White, Hatsch and Rosenbluth, taken singly or in combination, do not teach or suggest "wherein the feature indicative of process-related variation is at least one of (i) slope of edge intensity and (ii) logarithm of slope of edge intensity" as recited in claim 10. The Examiner cites paragraphs [0015, 0019 and 0099] of Rosenbluth as teaching the above-cited claim limitations. Office Action (10/23/2006), page 7. Appellants respectfully traverse.

Rosenbluth instead teaches that phase-shifting chrome or attenuated phase shift improves image sharpness by augmenting the rate of change in illumination amplitude across the edge of mask features. [0015]. Rosenbluth further teaches that methods are known for selecting the illumination directions incident on a given mask in ways that maximize the slope of image features, and that minimize CD nonuniformity between different features through superposition of multiple illumination directions. [0019]. Rosenbluth additionally teaches that the optimization in step 0 can be performed against the finite difference between adjacent dark and bright points across feature edges. [0099]. There is no language in the cited passages that teaches that the feature of the simulated structures indicative of process-related variation is at least one of (i) slope of edge intensity and (ii) logarithm of slope

of edge intensity. Therefore, the Examiner has not presented a *prima facie* case of obviousness in rejecting claim 10, since the Examiner is relying upon incorrect, factual predicates in support of the rejection. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1455 (Fed. Cir. 1998).

b. Claim 11 is patentable over White in view of Hatsch and in further view of Rosenbluth.

Appellants respectfully assert that White, Hatsch and Rosenbluth, taken singly or in combination, do not teach or suggest "a larger slope of edge intensity or logarithm of slope of edge intensity is indicative of a smaller process-related variation; and a smaller slope of edge intensity or logarithm of slope of edge intensity is indicative of a larger process-related variation" as recited in claim 11. The Examiner cites paragraphs [0019 and 0082] of Rosenbluth as teaching the above-cited claim limitations. Office Action (10/23/2006), page 7. Appellants respectfully traverse.

Rosenbluth instead teaches that methods are known for selecting the illumination directions incident on a given mask in ways that maximize the slope of image features, and that minimize CD nonuniformity between different features through superposition of multiple illumination directions. [0019]. Rosenbluth further teaches that the index r runs over sample points along the edges of the target patterns, for example, as indicated by points 604, 606, 608, 610, and 612 in Figure 6. [0082]. There is no language in the cited passages that teaches a larger slope of edge intensity or logarithm of slope of edge intensity is indicative of a smaller process-related variation. Neither is there any language in the cited passages that teaches a smaller slope of edge intensity or logarithm of slope of edge intensity is indicative of a larger process-related variation. Therefore, the Examiner has not presented a *prima facie* case of obviousness in rejecting claim 11, since the Examiner is relying upon incorrect, factual predicates in support of the rejection. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1455 (Fed. Cir. 1998).

c. Claim 19 is patentable over White in view of Hatsch and in further view of Rosenbluth

Appellants respectfully assert that White, Hatsch and Rosenbluth, taken singly or in combination, do not teach or suggest "providing feedback to a designer regarding how a given structure will print on a wafer as a function of at least one of (i) proximity of a structure to other structures, (ii) density of structures within a portion of the IC device design, (iii) orientation of a structure, (iv) placement of a structure within a portion of the IC device design, and (v) size of a structure with respect to other adjacent structures" as recited in claim 19. The Examiner cites paragraphs [0115, 0178, 0220 and 0224] of White as teaching the above-cited claim limitation. Office Action (10/23/2006), page 6. Appellants respectfully traverse.

White instead teaches that an integrated circuit typically includes multiple levels of materials that have been deposited, planarized, and selectively etched to reproduce circuitry defined by a computer-generated design. [0115]. White further teaches that lithography is a frequently repeated process step during the manufacture of ICs in which a pattern that defines the dimensions of the circuitry is transferred to a silicon wafer. [0115]. White further teaches that the layout file is transferred or uploaded to the computer where the extraction algorithm is running 311. [0178]. White additionally teaches that the layout information, which may include design and extraction data 601, predicated critical dimensions, and feature sizes 680, are loaded into the verification and correction component 800. [0220]. Furthermore, White teaches verifying discrete grid sizes greater than the minimum IC dimensions. [0224]. There is no language in the cited passages that teaches providing feedback to a designer regarding how a given structure will print on a wafer as a function of at least one of (i) proximity of a structure to other structures, (ii) density of structures within a portion of the IC device design, (iii) orientation of a structure, (iv) placement of a structure within a portion of the IC device design, and (v) size of a structure with respect to other adjacent structures. Therefore, the Examiner has not presented a *prima facie* case of obviousness in rejecting claim 19, since the Examiner is relying

upon incorrect, factual predicates in support of the rejection. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1455 (Fed. Cir. 1998).

VIII. CONCLUSION

For the reasons noted above, the rejections of claims 1-4, 6-20 and 31 are in error. Appellants respectfully request reversal of the rejections and allowance of claims 1-4, 6-20 and 31.

Respectfully submitted,

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CLAIMS APPENDIX

1. A method of designing an integrated circuit (IC) device having desired electrical characteristics, said method comprising:

providing an initial IC device design;

generating a layout representation corresponding to the initial IC device design;

simulating how structures within the layout representation will pattern on a wafer;

based on the simulating step, determining whether actual electrical characteristics associated with the initial IC device design sufficiently match the desired electrical characteristics, wherein the desired electrical characteristics include at least one of gain and switching speed; and

if the actual electrical characteristics associated with the initial IC device design do not sufficiently match the desired electrical characteristics, modifying the initial IC device design.

2. The method of claim 1, wherein the step of determining whether the actual electrical characteristics associated with the initial IC device design sufficiently match the desired electrical characteristics includes:

determining actual dimensions of structures within the layout representation based on the simulating step; and

determining the actual electrical characteristics associated with the actual dimensions of the structures within the layout representation.

3. The method of claim 2, wherein the actual electrical characteristics associated with the actual dimensions of the structures within the layout representation are determined using a look-up table.

4. The method of claim 2, wherein the actual electrical characteristics associated with the actual dimensions of the structures within the layout representation are

determined using an electrical modeling program in which the actual dimensions of the structures are input.

6. The method of claim 1, wherein the step of generating a layout representation corresponding to the initial IC device design includes minimizing the scale of the layout representation.

7. The method of claim 1, wherein the initial IC device design includes a desired relationship between at least two structures within the IC device design.

8. The method of claim 7, further comprising:

determining an amount of process-related variation associated with at least two structures within the layout representation of the IC device design.

9. The method of claim 8, wherein determining an amount of process-related variation associated with at least two structures within the layout representation includes:

simulating how structures within the layout representation will pattern on a wafer; and

measuring a feature of the simulated structures, said feature being indicative of process-related variation.

10. The method of claim 9, wherein the feature indicative of process-related variation is at least one of (i) slope of edge intensity and (ii) logarithm of slope of edge intensity.

11. The method of claim 10, wherein:

a larger slope of edge intensity or logarithm of slope of edge intensity is indicative of a smaller process-related variation; and

a smaller slope of edge intensity or logarithm of slope of edge intensity is indicative of a larger process-related variation.

12. The method of claim 9, said method further comprising:

measuring the feature indicative of process-related variation for one or more simulated structures over a process window of focus and intensity.

13. The method of claim 12, wherein the simulated structures are at different locations within the layout representation.

14. The method of claim 9, wherein simulating how structures within the layout representation will pattern on a wafer includes simulating how structures within the layout representation will pattern as a function of at least one of (i) proximity of a structure to other structures, (ii) density of structures within a portion of the IC device design, (iii) orientation of a structure, (iv) placement of a structure within a portion of the IC device design, and (v) size of a structure with respect to other adjacent structures.

15. The method of claim 9, further comprising:

determining whether at least a portion of the IC device design is optimized with respect to process-related variations.

16. The method of claim 15, further comprising:

if a portion of the IC device design is not optimized with respect to process-related variations, modifying at least a portion of the IC device design.

17. The method of claim 16, wherein modifying at least a portion of the IC device design includes modifying at least one of (i) proximity of a structure to other structures, (ii) density of structures within a portion of the IC device design, (iii) orientation of a structure, and (ii) (iv) placement of a structure within a portion of the IC device design, and (v) size of a structure with respect to other adjacent structures.

18. The method of claim 9, wherein the process-related variations include variations caused by at least one of (i) mask generation, (ii) wafer patterning, (iii) pre-patterning processing, and (iv) post-patterning processing.

19. The method of claim 11, further comprising:

providing feedback to a designer regarding how a given structure will print on a wafer as a function of at least one of (i) proximity of a structure to other structures, (ii) density of structures within a portion of the IC device design, (iii) orientation of a structure, (iv) placement of a structure within a portion of the IC device design, and (v) size of a structure with respect to other adjacent structures.

20. An integrated circuit (IC) device designed by the method of claim 1.

31. A computer-implemented method in which an initial integrated circuit (IC) device design is provided, said method comprising:

generating a layout representation corresponding to the initial IC device design;

simulating how structures within the layout representation will pattern on a wafer;

based on the simulating step, determining an amount of process-related variation in how at least a portion of the layout representation will pattern on a wafer; and

determining whether the layout representation will pattern as an IC device having desired electrical characteristics, wherein the desired electrical characteristics include at least one of gain and switching speed.

EVIDENCE APPENDIX

No evidence was submitted pursuant to §§1.130, 1.131, or 1.132 of 37 C.F.R. or of any other evidence entered by the Examiner and relied upon by Appellants in the Appeal.

RELATED PROCEEDINGS APPENDIX

There are no related proceedings to the current proceeding.